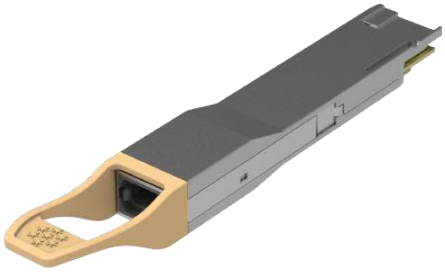
400G QSFP56 DD SR8 Optical Transceiver Module

NQS-M400-L001 (MPO24)/NQS-M400-L001 (MPO16)

Features



8 channels full-duplex transceiver modules

Transmission data rate up to 53Gbps per channel

8x53Gbps PAM4 transmitter and PAM4 receiver

8 channels 850nm VCSEL array

8 channels PIN photo detector array

Internal CDR circuits on both receiver and transmitter channels

Power consumption <10W

Hot Pluggable QSFP DD form factor and Compliant with CMIS

Maximum link length of 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF with FEC

MPO24 PC connector receptacle (B version)

MPO16 APC connector receptacle (C version)

Built-in digital diagnostic functions

Operating case temperature 0℃ to +70℃

3.3V power supply voltage

RoHS compliant (lead free)

Applications

IEEE 802.3cd 200GBASE-SR4

Description

NQS-M400-L001 is an Eight-Channel, Pluggable, Parallel, Fiber-Optic QSFP Double Density for 2x200 Gigabit Ethernet Applications. This transceiver is a high-performance module for short-range multi-lane data communication and interconnection applications. It integrates eight data lanes in each direction with 8x26.5625GBd. Each lane can operate at 53.125Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber with FEC. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76-contact edge type connector. The optical interface uses a MTP24/MPO24 PC connector (or MPO16/MTP16 APC connector). The Common Management Interface Specification (CMIS) for QSFP DD modules, this module incorporates proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

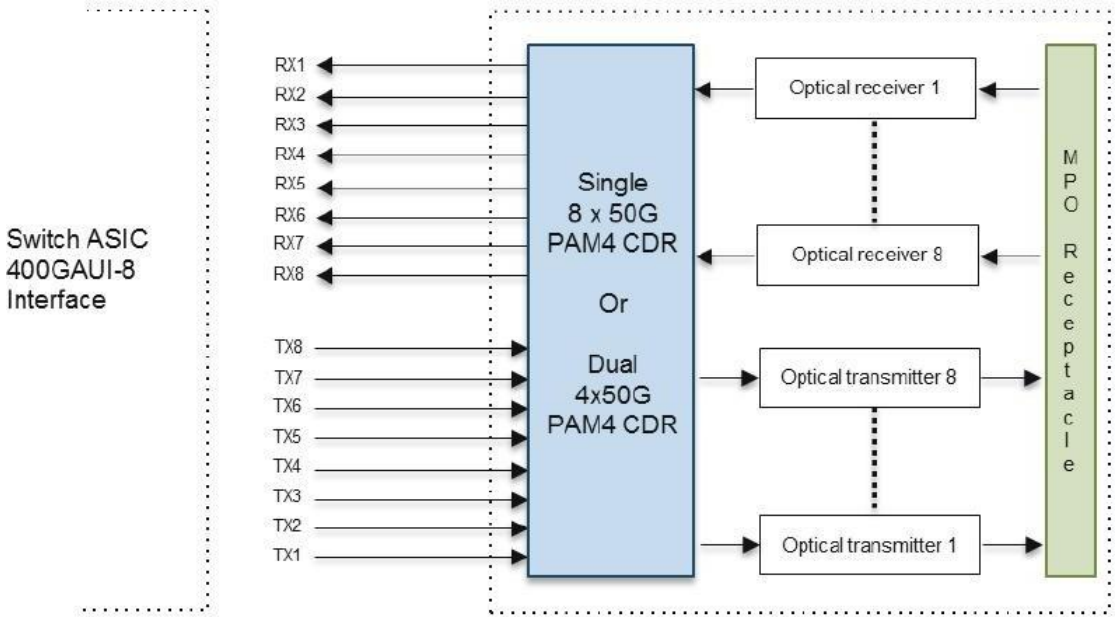


Figure1. Module Block Diagram

2x200GBASE-SR4 QSFP DD is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I^2C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	℃
Case Operating Temperature	Top	0	70	℃
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	℃
Data Rate Per Lane	fd		26.5625		GBd
Humidity	Rh	5		85	%
Power Dissipation	Pm			10	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage	ΔVin			900	mVp-p
Differential output voltage	ΔVout			900	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			2.4E-4	-
Near-end Eye Width at 10^-6 probability(EW6)		0.265			UI
Near-end Eye Height at 10^-6 probability(EH6)		70			mV
Far-end Eye Width at 10^-6 probability(EW6)		0.20			UI
Far-end Eye Height at 10^-6 probability(EH6)		30			mV
Near-end Eye Linearity		0.85			-

Note:

1. BER=2.4E-4; PRBS31Q@26.5625GBd. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN. Differential output voltage amplitude is measured between RxnP and RxnN

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.6	nm	-
Average launch power, each lane	Pout	-6	-	4	dBm	-
Optical Modulation Amplitude (OMAouter), each lane	OMA	-4.5		3	dBm	-
Transmitter and dispersion eye closure(TDEC),each lane	TDEC			4.5	dB	
Extinction Ratio	ER	3	-	-	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Receiver						
Centre Wavelength	λc	840	850	860	nm	-
Receiver Sensitivity in OMAout	RXsen	-6.5		-3.4	dBm	1
Stressed Receiver Sensitivity in OMAout				-3	dBm	1
Maximum Average power at receiver , each lane input, each lane				4	dBm	-
Minimum Average power at receiver , each lane		-7.9			dBm	
Receiver Reflectance				-12	dB	-
LOS Assert		-10			dBm	-
LOS De-Assert – OMA				-7.5	dBm	-
LOS Hysteresis		0.5			dB	-

Note:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Pin Description

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

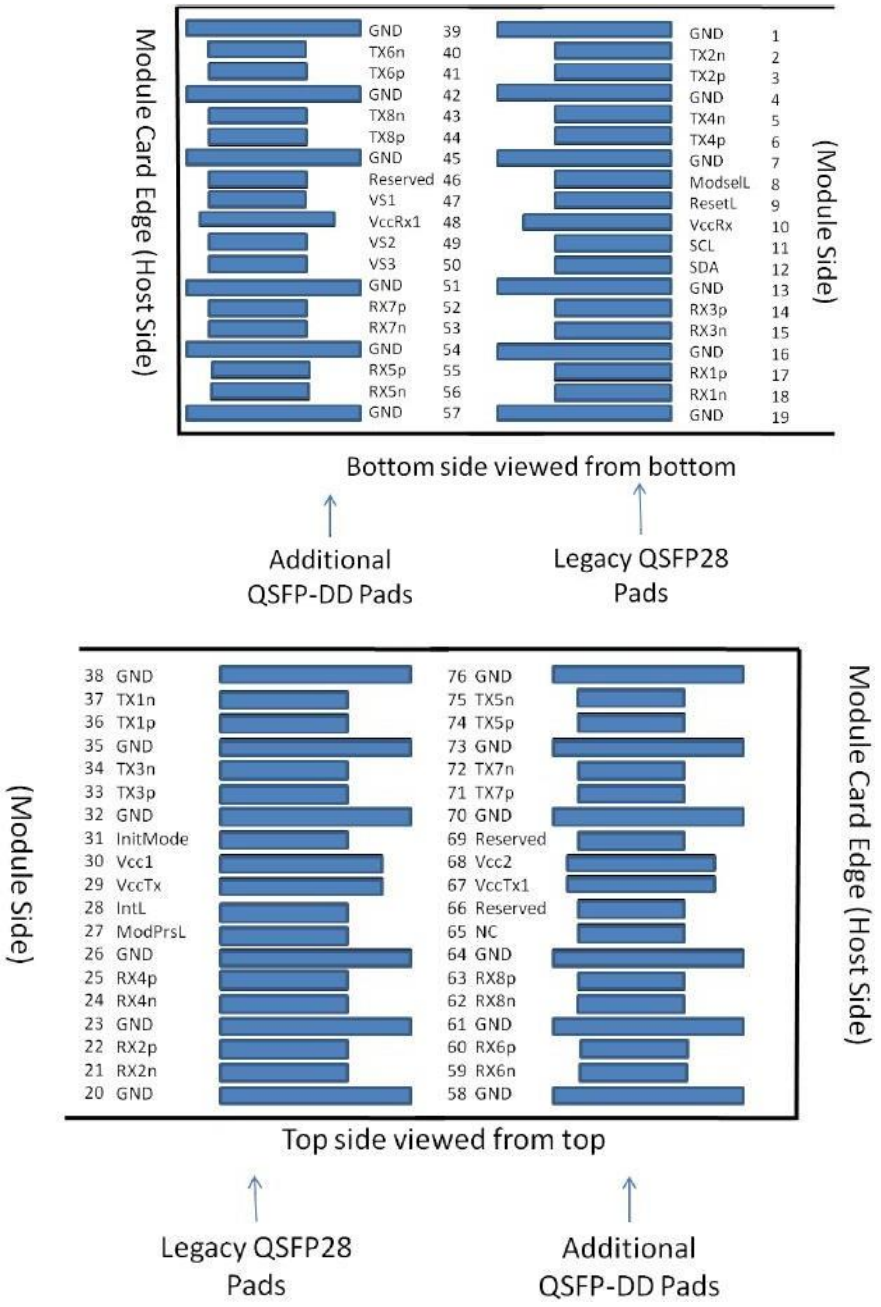


Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

InitMode Pin

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in Section 7.5. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for signal description.

ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

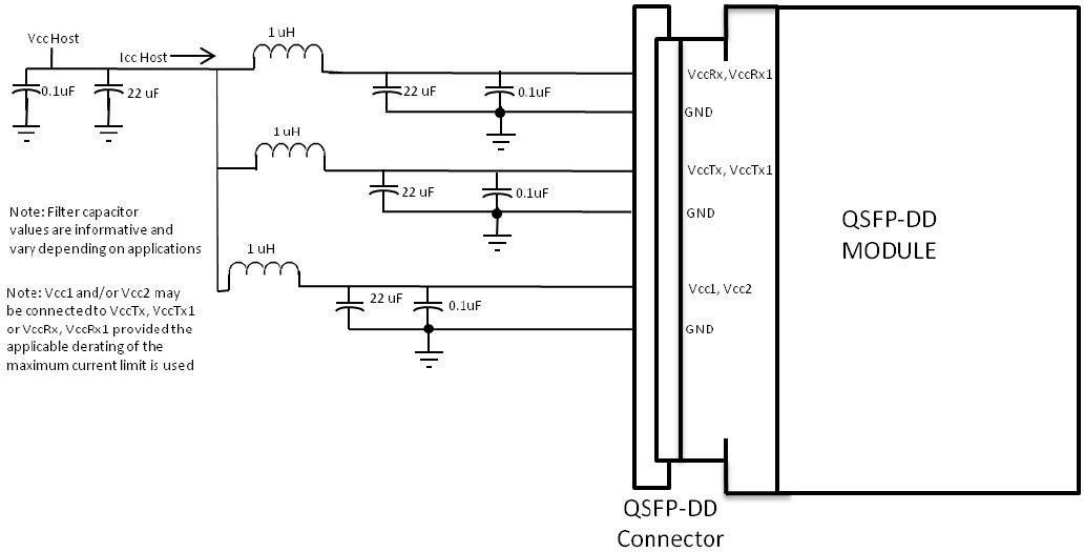
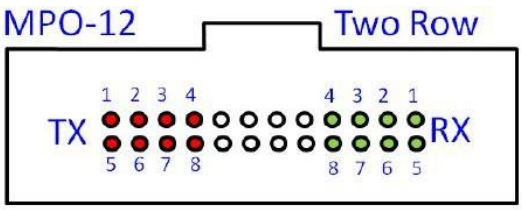


Figure3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The optical interface port is a male MPO24(MTP24) PC connector for GQD-MPO401-SR8CB



The optical interface port is a male MPO16(MTP16) APC connector for GQD-MPO401-SR8CC

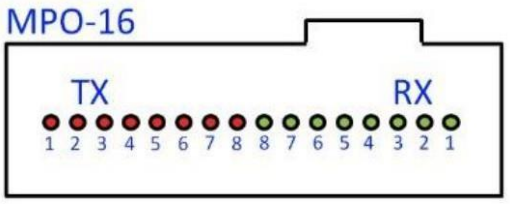


Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE

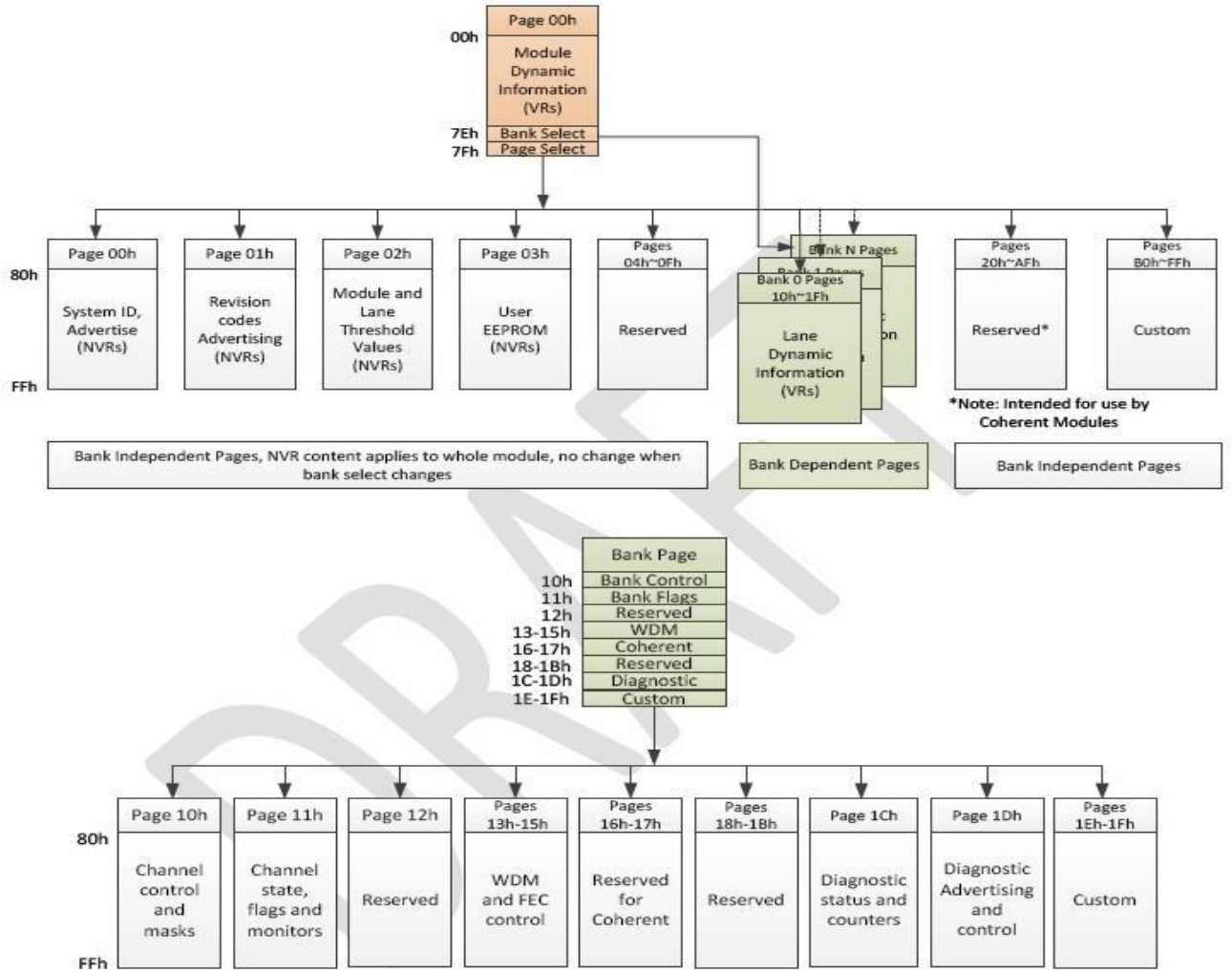
Digital diagnostics monitoring function is available on all QSFP DD products. A 2-wire serial interfaceprovides user to contact with module.

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages.This structure supports a flat 256 byte memory for passive copper cables and permits timely access to addresses in the lower page, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. Upper pages 00-02 all contain static, non-volatile advertising registers. Upper page 01 provides revision codes and advertising registers that indicate the capabilities of the module. Upper page 02 provides thresholds for monitored functions. Upper page 03 provides a user read/write space. The lower page and upper page 00 are required for passive copper cables and are always implemented. In addition, upper pages 1, 2 and bank 0 pages 10h and 11h are required for active modules. See CMIS Document Table 40 for details regarding the implementation of optional upper pages and the bank pages.

Bank pages are provided to provide the ability to support modules with more than 8 lanes. Bank 0 provides lane-specific registers for the lower 8 lanes. Each additional bank provides support for an additional 8 lanes.

Reserved bytes are for future use and shall not be used and shall be set to 0. Other organizations shall contact the managing organization or the editor of this document to request allocations of registers. The use of custom bytes is not restricted and may be vendor defined. The use of registers defined as custom may be subject to additional agreements between module users and vendors.



Mechanical Dimensions

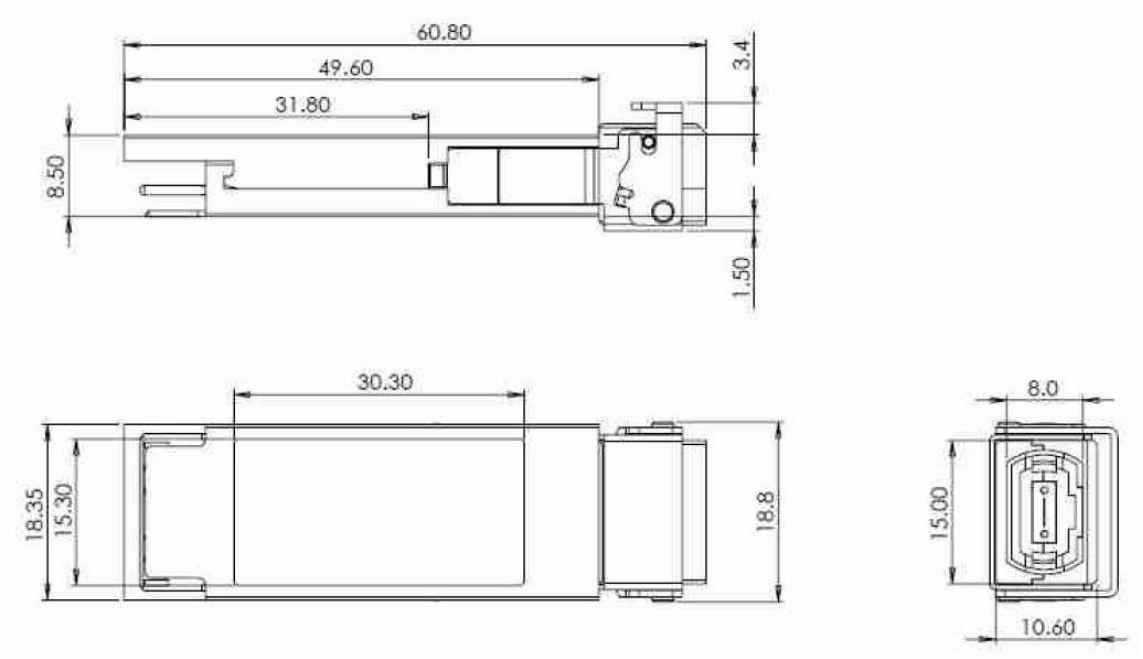


Figure6. Mechanical Specifications

Regulatory Compliance

NQD-MDO401-SR8C(B/C) transceivers are Class 1 Laser Products. They are compliant with the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP DD MAS Rev4.0
2. CMIS V4.0
3. IEEE802.3cd 200GBASE-SR4
4. OIF CEI-56G-VSR-PAM4

Ordering information

Part Number	Product Description
NQS-M400-L001	QSFP DD, 2x200GBASE-SR4, 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF, with DSP Power consumption <10W, MPO24(MTP24) PC connector
NQS-M400-L001	QSFP DD, 2x200GBASE-SR4, 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF, with DSP Power consumption <10W, MPO16(MTP16) APC connector