40G QSFP+ Active Optical Cables
P/N: NQS-MDO400-XXXC (xxx: 001 to 300)

Features

4 channels full-duplex 850nm parallel active optical cable

Transmission data rate up to 10.3Gbps per channel

4 channels 850nm VCSEL array

4 channels PIN photo-detector array

SFF-8436 QSFP+ compliant

Hot-pluggable electrical interface

Differential AC-coupled high-speed data interface

Up to 300m on OM3 MMF

Low power consumption < 1.5W

Operating case temperature range 0°C to +70°C

3.3V power supply voltage

RoHS 6 compliant

Applications

IEEE 802.3ba 40GBASE-SR4

InfiniBand SDR/DDR/QDR

Description

The 40G QSFP+ Active Optic Cables (AOCs) are direct-attach fiber assemblies with QSFP+ connectors, compliant with the QSFP MSA, 40G Ethernet IEEE 802.3ba 40GBASE-SR4, and InfiniBand SDR/DDR/QDR standards. They are suitable for short distances and offer a cost-effective solution to connect within racks and across adjacent racks. The 40G QSFP+ AOC is an assembly of 4 full-duplex lanes and each lane is capable of transmitting data at rates up to 10.3Gb/s, providing an aggregated rate of 41.2Gb/s. The length is up to 300 meters using OM3 MMF.
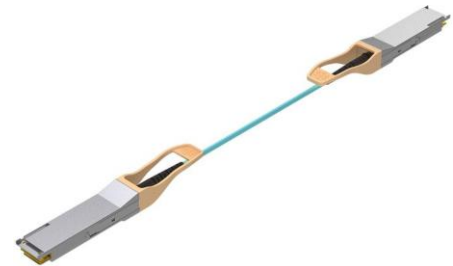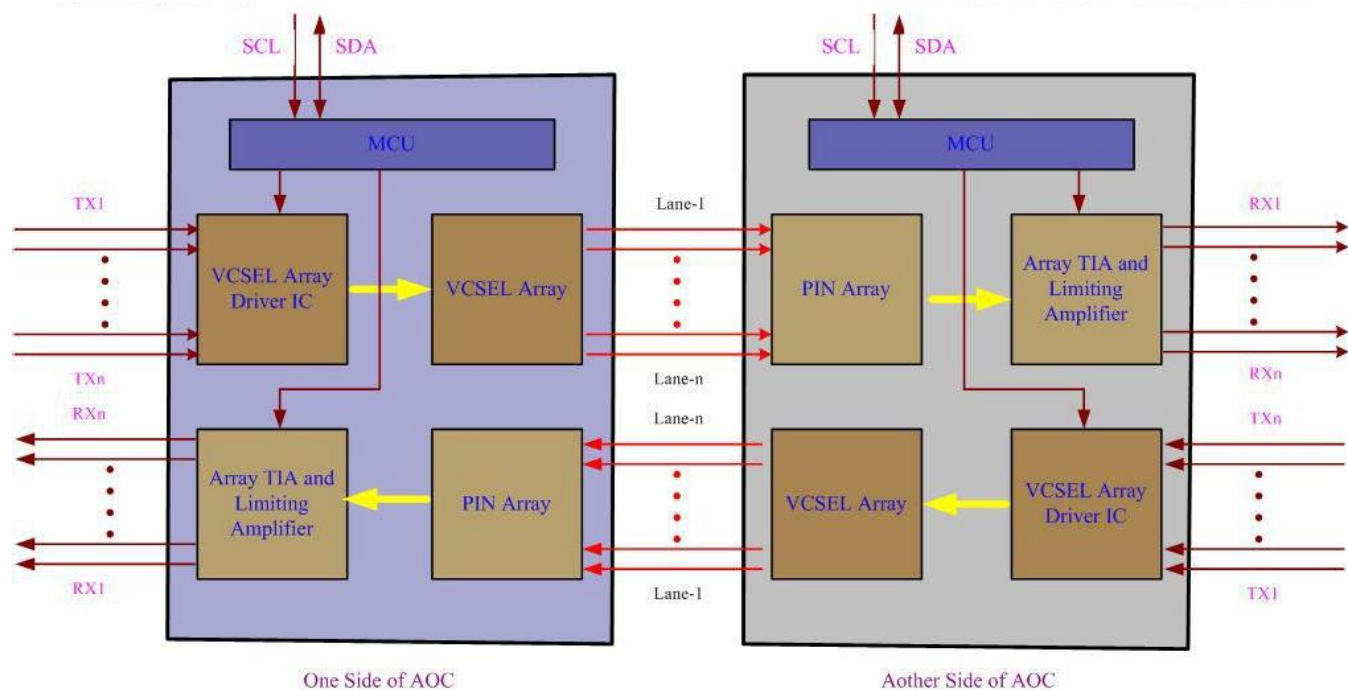
Figure1. Module Block Diagram

The 40G QSFP+ AOC is a kind of parallel transceiver optics assembly. VCSEL and PIN array package is key technique, though I^{2}C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd	2.5	10.3	11.1	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			1.5	W
Fiber Bend Radius	Rb	3			cm

Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	300		1100	mVp-p
Differential output voltage amplitude	ΔVout	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BR			E-12	
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Note：
1. BER=10^-12; PRBS 2^31-1@10.3125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN
3. Differential output voltage amplitude is measured between RxNP and RxnN

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.65	nm	-
Average launch power, each lane	Pout	-7.6	-	2.4	dBm	-
Difference in launch power between any two lanes (OMA)				4	dB	-
Extinction Ratio	ER	3	-	-	dB	-
Peak power, each lane				4	dBm	-
Transmitter and dispersion penalty (TDP), each lane	TDP			3.5	dB	-
Average launch power of OFF transmitter, each lane				-30	dBm	-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4					Hit Ratio = 5x10-5
Receiver						
Centre Wavelength	λc	840	850	860	nm	-
Stressed receiver sensitivity in OMA, each lane				-5.4	dBm	1
Maximum Average power at receiver input, each lane				2.4	dBm	-
Receiver Reflectance				-12	dB	-
Peak power, each lane				4	dBm	-
LOS Assert		-30			dBm	-
LOS De-Assert – OMA				-7.5	dBm	-

| | | | | LOS Hysteresis | | 0.5 | | | dB | - |

Note：

1．Measured with conformance test signal at TP3 for BER = 10e-12

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.

Top Side		Bottom Side	
38	GND	GND	1
37	TX1n	TX2n	2
36	TX1p	TX2p	3
35	GND	GND	4
34	TX3n	TX4n	5
33	TX3p	TX4p	6
32	GND	GND	7
31	LPMode	ModSelL	8
30	Vcc1	ResetL	9
29	VccTx	VccRx	10
28	IntL	SCL	11
27	ModPrsL	SDA	12
26	GND	GND	13
25	RX4p	RX3p	14
24	RX4n	RX3n	15
23	GND	GND	16
22	RX2p	RX1p	17
21	RX2n	RX1n	18
20	GND	GND	19

Card Edge

Top Side
Viewed from Top

Bottom Side
Viewed from Bottom
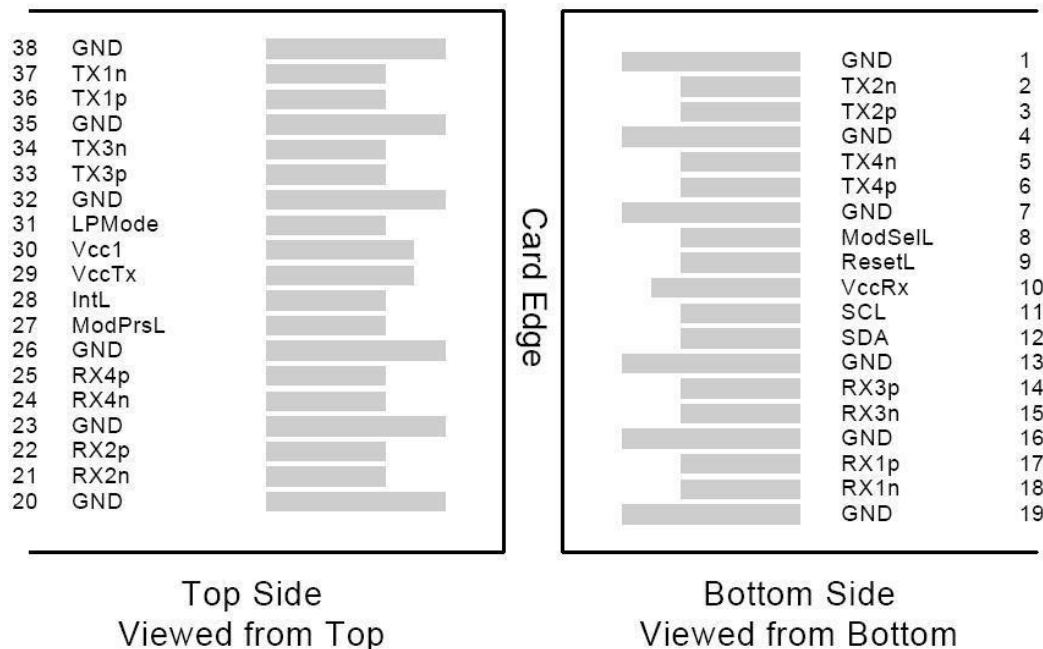
Figure2. Electrical Pin-out Details

ModSelL
Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin
QSFP AOC operate in the low power mode (less than 1.5 W power consumption) This pin
active high will decrease power consumption to less than 1W.
**ModPrsL Pin**
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low"
when the module is inserted and deasserted "High" when the module is physically absent from the host
connector.
IntL Pin
IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the
host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is
an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.
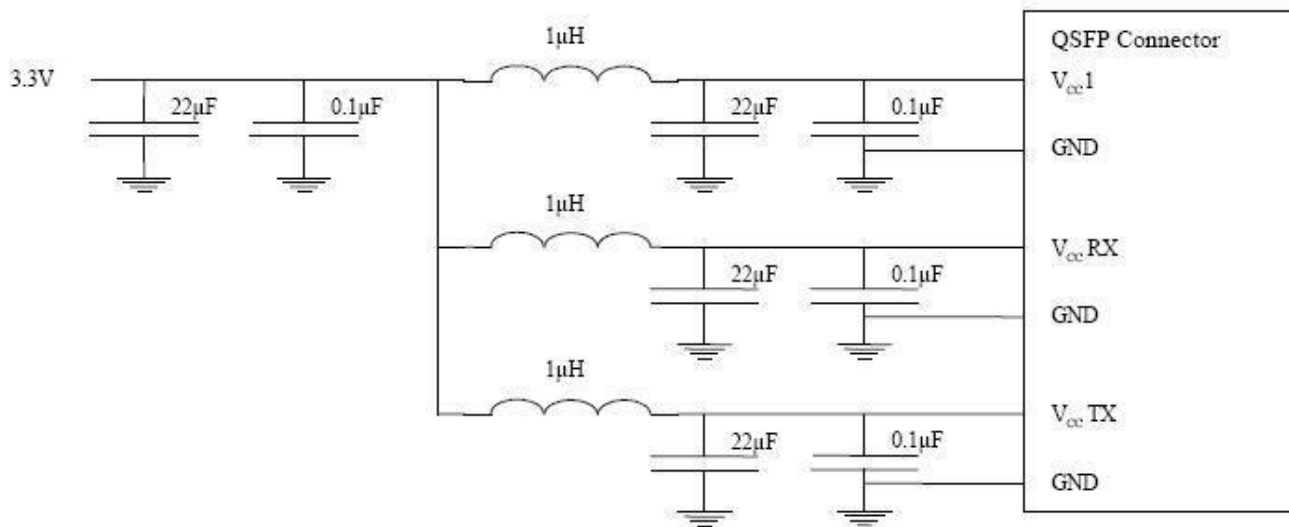
Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)
Digital diagnostics monitoring function is available on all QSFP AOCs. A 2-wire serial interface provides user to
contact with module.
The structure of the memory is shown in Figure 4. The memory space is arranged into a lower, single page,
address space of 128 bytes and multiple upper address space pages. This structure permits timely access to
addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as
serial ID information and threshold settings, are available with the Page Select function.
The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to
enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been
asserted, the host can read out the flag field to determine the affected channel and type of flag.
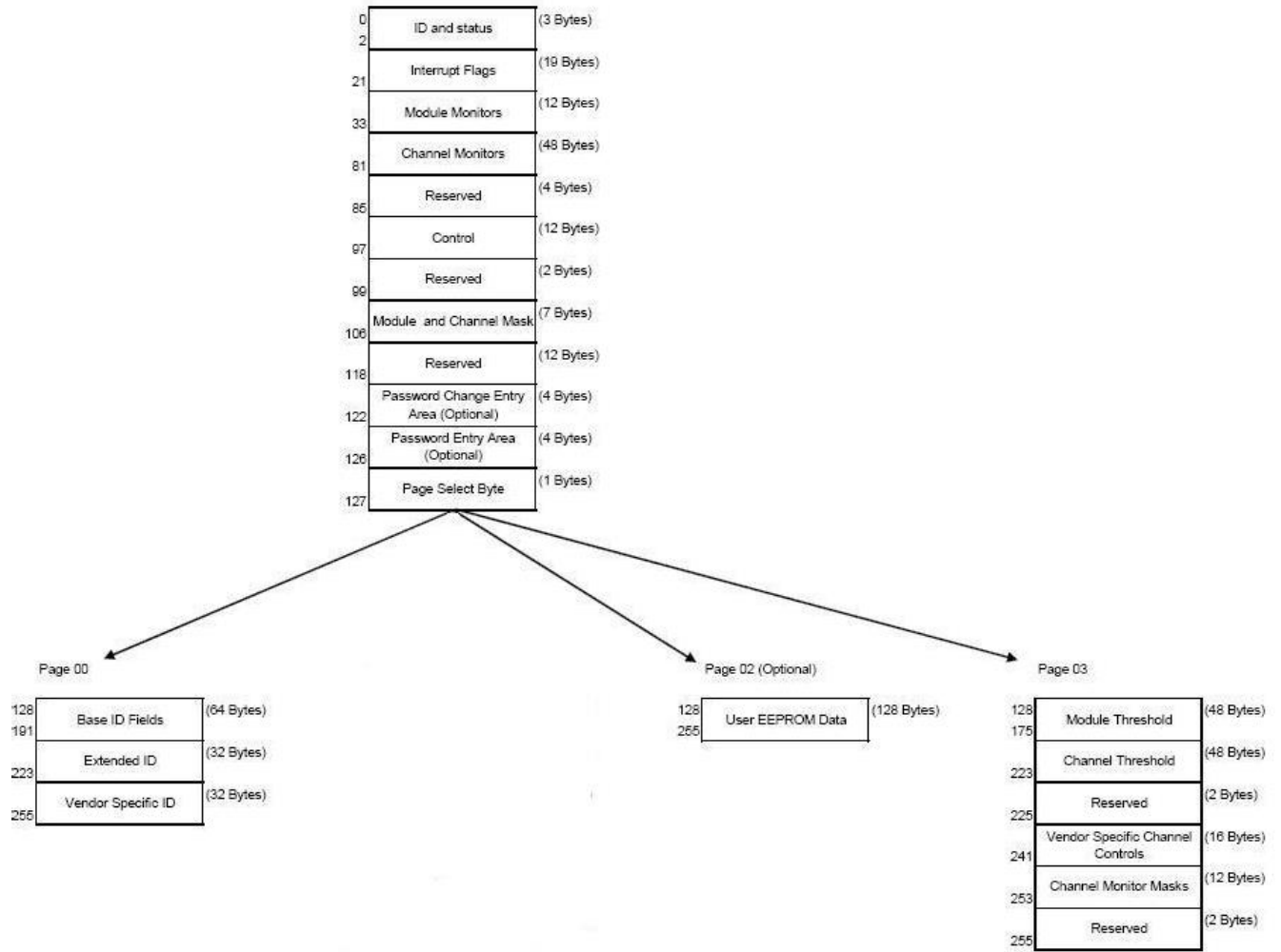
2-wire serial address, 1010000x (A0h)"

Offset	Block	Size
0 – 2	ID and status	(3 Bytes)
2 – 21	Interrupt Flags	(19 Bytes)
21 – 33	Module Monitors	(12 Bytes)
33 – 81	Channel Monitors	(48 Bytes)
81 – 85	Reserved	(4 Bytes)
85 – 97	Control	(12 Bytes)
97 – 99	Reserved	(2 Bytes)
99 – 106	Module and Channel Mask	(7 Bytes)
106 – 118	Reserved	(12 Bytes)
118 – 122	Password Change Entry Area (Optional)	(4 Bytes)
122 – 126	Password Entry Area (Optional)	(4 Bytes)
126 – 127	Page Select Byte	(1 Bytes)

Page 00

Offset	Block	Size
128 – 191	Base ID Fields	(64 Bytes)
191 – 223	Extended ID	(32 Bytes)
223 – 255	Vendor Specific ID	(32 Bytes)

Page 02 (Optional)

Offset	Block	Size
128 – 255	User EEPROM Data	(128 Bytes)

Page 03

Offset	Block	Size
128 – 175	Module Threshold	(48 Bytes)
175 – 223	Channel Threshold	(48 Bytes)
223 – 225	Reserved	(2 Bytes)
225 – 241	Vendor Specific Channel Controls	(16 Bytes)
241 – 253	Channel Monitor Masks	(12 Bytes)
253 – 255	Reserved	(2 Bytes)

Figure4. QSFP Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure5. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure6. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand[†]
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure7. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[2], hot plug or rising edge of Reset until the module is fully functional[3] This time does not apply to non-Power Level 0 modules in the Low Power State
Reset Init Assert Time	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[2] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[2] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[3]
LPMode Assert Time	ton_LPMode	100	µs	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level 1
LPMode Deassert Time	Toff_LPMode	300	ms	Time for deassertion of LPMode (Vin:LPMode=Vil) until module is fully functional[3,5]
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	µs	Time from clear on read[4] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set (value=1b) and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set(value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value=0b)[1] until associated IntlL operation resumes
Application or Rate Select Change Time	t_ratesel	100	µs	Time from change of state of Application or Rate Select Bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value=1b)[1] until module power consumption enters lower Power Level 1
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared(value=0b)[1] until the module is fully functional[3]

![НПО "ТЕЛЕКОМ"]

Note：
1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Figure8. Timing Specifications

Mechanical Dimensions
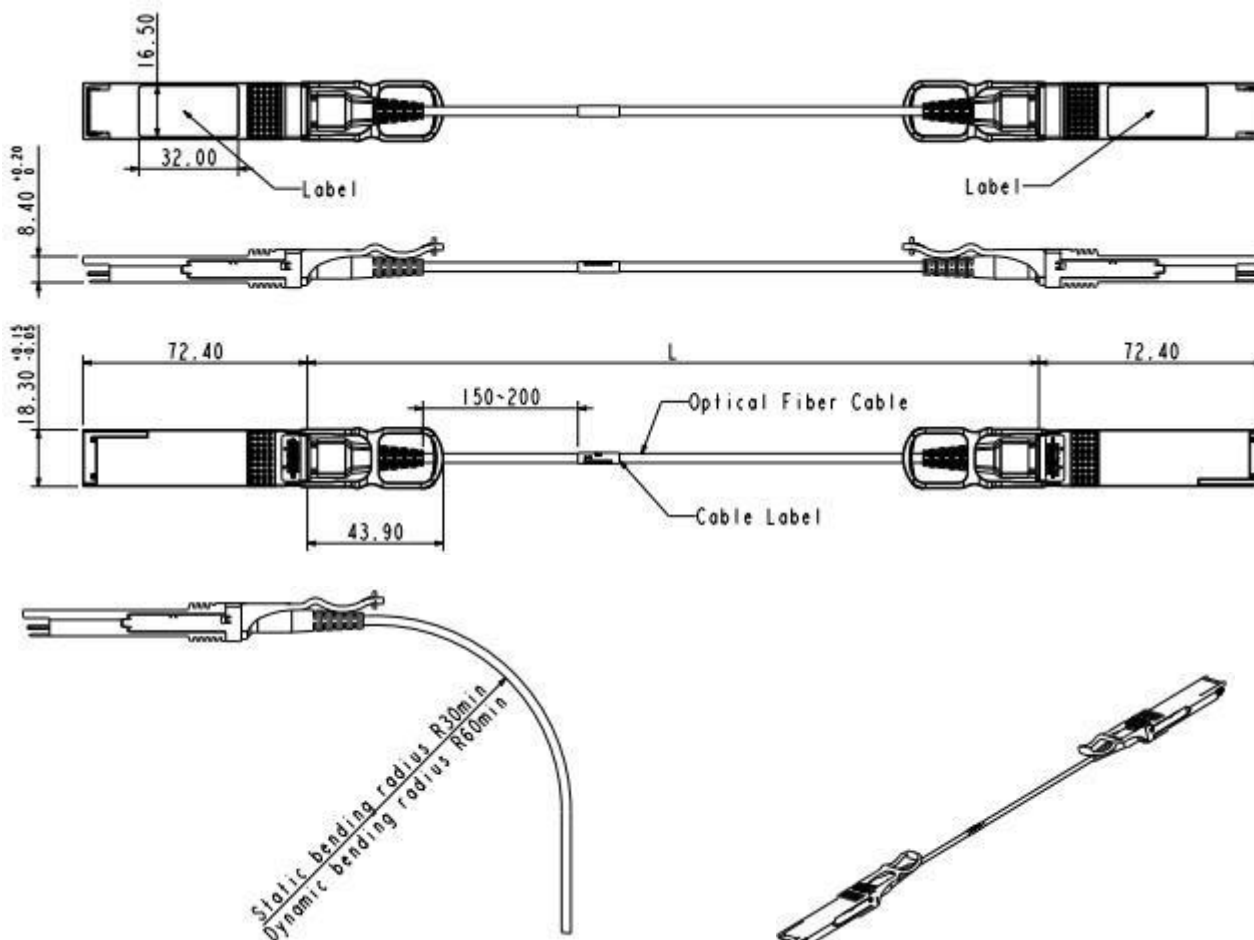
Figure9. Mechanical Specifications

Ordering information

Part Number	Product Description
NQS-MDO400-XXXC	**xxx**=different cable lengths on OM3 Multimode Fiber (MMF)
XX(X)	**Cable Length** on OM3 Multimode Fiber (MMF)
03	**003**=3m
05	**005**=5m
10	**010**=10m
20	**020**=20m
50	**050**=50m
300	**300**=300m

References
1. SFF-8436 QSFP+
2. Infiniband IB-4x-SX, IB-4x-DDR-SX, IB-4x-QDR-SX
3. Ethernet 40GBASE-SR4