Features

QSFP28 MSA package with simplex LC connector

Compliant to 100G Lamda MSA 100G-LR1-20 Optical Specifications

Interoperable with IEEE 802.3cu

Lane signaling rate 53.125GBd with PAM4

High speed I/O electrical interface

Two Wire Serial Interface with Digital Diagnostic Monitoring

Operating case temperature range 0°C to +70°C

Support KP4 FEC inside the module and KP4 FEC shutdown

Reaches up to 20km on SMF

Maximum power consumption 4.5W

3.3V power supply voltage

compliant to RoHS2.0

Class 1 Laser

Applications

100 Gigabit Ethernet

Data Center

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Max.	Unit
Storage temperature（case）	Tstg	-	-40	+85	℃
Relative Humidity	RH	Non-condensing	5	85	%
Supply voltage	VCC		0	3.6	V
Low speed signalvoltage range			-0.3	4.0	V
Damage threshold	Pin	Average		5.5	dBm
ESD Sensitivity		—		±500V for RF ±2kV for others	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tcase	0	-	70	ºC
Supply Voltage	VCC	3.135	3.3	3.465	V
Relative Humidity	RH	5	-	85	%
Power Dissipation	PD	-	-	4.5	W
Data Rate (optical)	DRO	-	103.125	106.25	Gbps
Data Rate (Electrical)	DRE	-	25.78	26.5625	Gbps
Operating Link Distance	LD	-	-	20	Km

Optical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmitter							
Data Rate				103.125	106.25	Gbps	
Data ratevariation			-100		+100	ppm	
Lane center wavelength			1264.5	1271	1277.5	nm	
			1324.5	1331	1377.5	nm	
Launch powerPer lane	Peach		-0.2		6.6	dBm	1，2
Optical modulation amplitude perlane	POMA		2.8 1.4+TDECQ		6.8	dBm	3
Transmitter and Dispersion eyeclosure	TDECQ				3.6	dBm	
Optical Extinction Ratio	ER		3.5			dB	
Side mode Suppression ratio	SMSR		30			dB	
Launch power of OFF Transmitterper lane					-30	dBm	
Relative Intensity Noise	RIN				-136	dB/Hz	
Optical returnloss tolerance					15.6	dB	
Transmitter reflectance					-26	dB	4
Receiver							
Data Rate				103.125	106.25	Gbps	
Data rate variation			-100		+100	Ppm	
Lane center wavelength			1324.5	1331	1377.5	nm	
			1264.5	1271	1277.5	nm	
Damage threshold	Rdam		7.6			dBm	5
Average receiver power	Rpow		-10		6.6	dBm	6
Receiver power(OMA) perlane	Rovl				6.8	dBm	
Receiver sensitivity (OMA), (max)	SENeach				-7.6 -9 + TECQ	dBm	7
Stressed Sensitivity per lane	SRS				-5.4	dBm	8
Receiver reflectance					-26	dB	
LOSS assert			-26		-12	dBm	
LOSS de-assert					-10	dBm	
Conditions of stressed receiver sensitivity test:							
Stressed eye closure for PAM4 (SECQ),					3.6	dB	8

Note1. As the total average launch power limit has to be met, not all of the lanes can operate at the maximum average launch power, each lane.

Note2. Average launch power, each lane(min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value can not be compliant: however, a value above this does not ensure compliance.

Note3. For TDECQ＜1.4dB， the OMAouter(min) is 2.8dB.For TDECQ 1.4 dB ≤TDECQ≤ TDECQ (max),the OMAouter(min) is 1.4+TDECQ.

Note4. Transmitter reflectance is defined looking into the transmitter.

Note5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

Note6. Average receiver power, each lane(min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note7. Measured with conformance test signal at TP3 for the BER specified in 《100G-FR and 100G-LR1 Technical Specifications Rev 2.0》.For TECQ < 1.4 dB,receiver sensitivity (OMA_{outer}) (max) is -7.6dB.
For TECQ 1.4 dB ≤ TECQ ≤ TECQ (max),receiver sensitivity (OMA_{outer}) (max) is -9 + TECQ dB.

Note8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristicsof the receiver.

Electrical Specifications

Transmitter (Module Input)					
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**
Input Differential Impedance	Rin	-	100	-	Ohm
Differential termination mismatch (max)	D-mismatch	-	-	10	%
Differential Data Input Amplitude	VIN,P-P	-	-	900	mVpp
LPMode, Reset and ModSelL	VIL	-0.3	-	0.8	V
	VIH	2.0	-	VCC+0.3	V
Receiver (Module Output)					
Output Differential Impedance	Rout	-	100	-	Ohm
Differential termination mismatch (max)	D-mismatch	-	-	10	%
Differential Data Output Amplitude	VOUT,P-P	-	-	900	mVpp
ModPrsL and IntL	VOL	0	-	0.4	V
	VOH	VCC-0.5	-	VCC+0.3	V

Pin layout

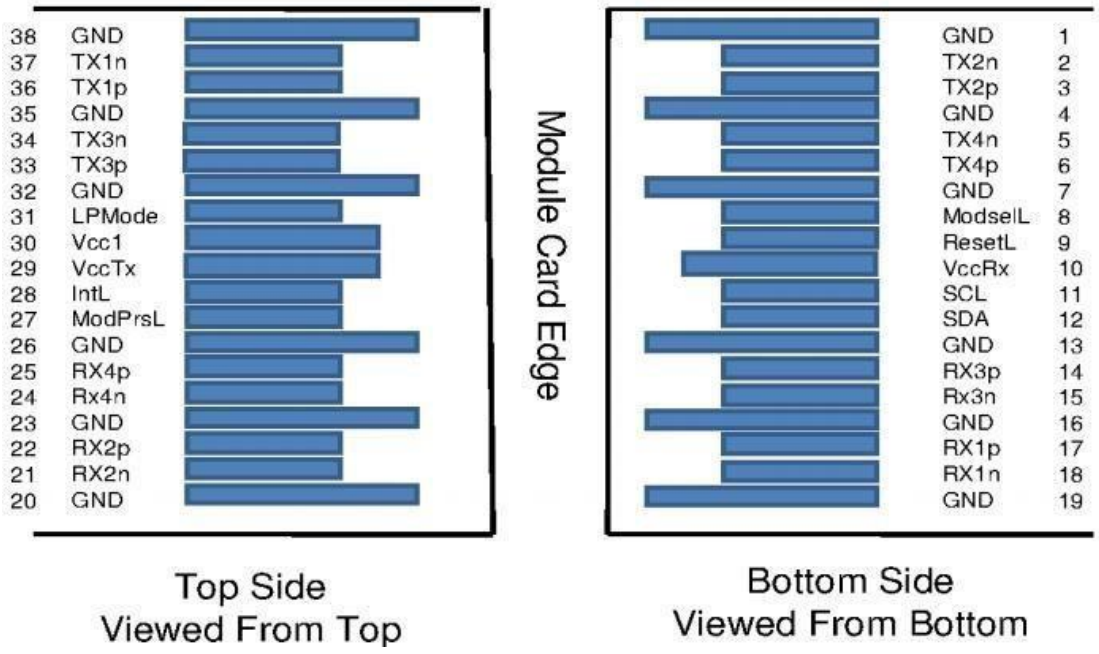

Figure1 Top Side and Bottom Side of QSFP28

Pin Definitions

Pin no.	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	3
9	LVTLL-I	ResetL	Module Reset	4
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	

23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL/RX_LOS	Interrupt/Rx LOS	5
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power mode/Tx Disable	5
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Note1.GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential.
unless otherwise noted. Connect these directly to the host board signal common ground plane.

Note2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power suppliers and shall beapplied concurrently. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Note3.Timing for SCL, SDA and ModSelL shall comply with the common management interface document SFF-8636 and SFF-8679.

Note4.The QSFP28 module must support hardware reset operation.

Note5.Two Multi-Purpose PIN for supporting Tx_DIS and Rx_LOS function in the 100G QSFP28 module.The IIC interface must function normally when the QSFP28 module is in the LP mode.

Host Board Power Supply Filtering

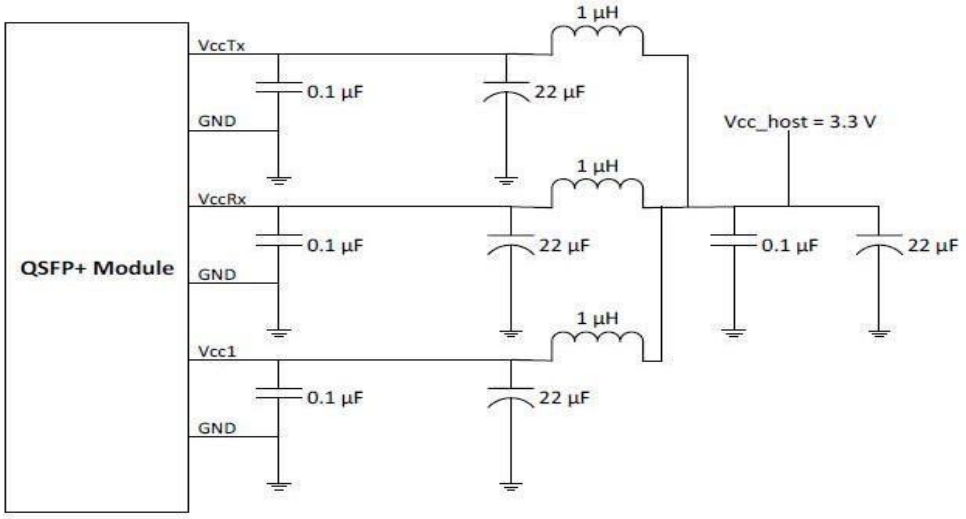

Figure2 Recommended host board power supply filtering

Mechanical Specifications

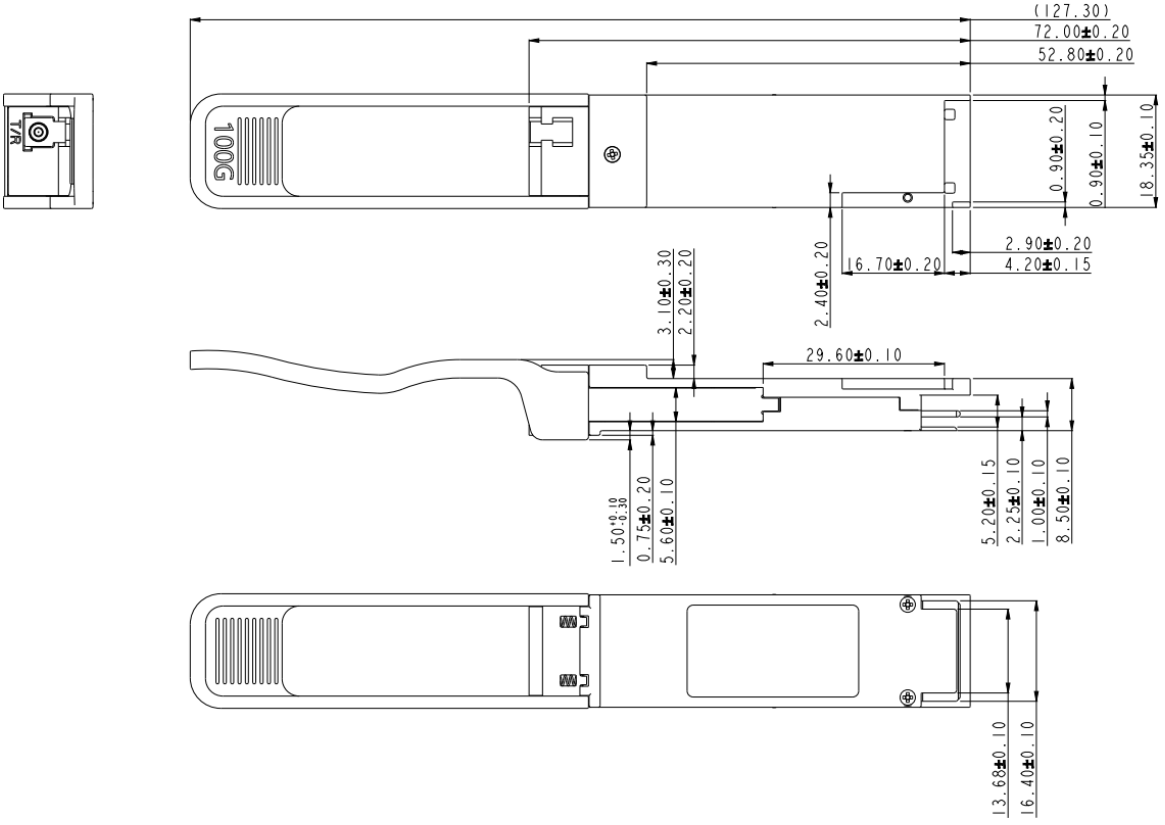

Figure3 100G LR1 BIDI QSFP28 Mechanical Dimensions

Register Application

Table 9-3 FEC and PRBS register requirements

03h	Bits	Name	Description
230	7	Host-Side FEC enable	0b: disable 1b:enable. Default=0
	6	Media-Side FEC enable	0b: enable 1b:disable. Default=0
	5-0	Reserved	

13h	Value	Name	Description
156	00h	PRBS31	Host/media sides PRBS generator and checker supported
	02h	PRBS23	
	04h	PRBS15	
	06h	PRBS13	
	08h	PRBS9	
	0ah	PRBS7	
	0ch	SSPRQ	Only support media side PRBS generator
13h	Bits	Name	Description
144	7-4	Reserved	1b=Enable generator 0b=disable generator
	3	Host side generator lane4 enable	
	2	Host side generator lane3 enable	
	1	Host side generator lane2 enable	
	0	Host side generator lane1 enable	
148	7-4	Host side generator lane2 pattern select	Selected pattern to be generated on each lane,See table 8-2 for pattern coding
	3-0	Host side generator lane1 pattern select	
149	7-4	Host side generator lane4 pattern select	
	3-0	Host side generator lane3 pattern select	
160	7-4	Reserved	1b=Enable generator 0b=disable generator
	3	Host side checker lane4 enable	
	2	Host side checker lane3 enable	
	1	Host side checker lane2 enable	
	0	Host side checker lane1 enable	

164	7-4	Host side checker lane2 pattern select	Selected pattern on each lane,See table 8-2 for pattern coding
	3-0	Host side checker lane1 pattern select	
165	7-4	Host side checker lane4 pattern select	
	3-0	Host side checker lane3 pattern select	
152	7-1	Reserved	0
	0	Media side generator lane1 enable	1b=Enable generator 0b=disable generator
156	7-4	Reserved	0
	3-0	Media side generator lane1 pattern select	Selected pattern to be generated on each lane,See table 8-2 for pattern coding
168	7-1	Reserved	0
	0	Media side checker lane1 enable	1b=Enable generator 0b=disable generator
172	7-4	Reserved	0
	3-0	Media side checker lane1 pattern select	Selected pattern on each lane,See table 8-2 for pattern coding

Table 9-4 BER check register requirements

14h	Lane	Description
192-193	Host side BER,lane1	BER in unsigned floating point 11.5 format as per
194-195	Host side BER,lane2	SFF8636,Error Figures section 6.7.4.4(Big Endian), Value=m*10^(s-24),m=mantissa,s=exponent Non Zero Range is 1.000E-24 to 2.047E+10. For Example,BER=0x6A84 Bit15-bit11:Exponent; bit10-bit0:mantissa S=13,m=0x284=644,value=644*10^(13-24),so BER is 6.44E-9
196-197	Host side BER,lane3	
198-199	Host side BER,lane4	
200-201	Reserved	
202-203	Reserved	
204-205	Reserved	
206-207	Reserved	
208-209	Media side BER,lane1	
210-211	Reserved	
212-213	Reserved	
214-215	Reserved	
216-217	Reserved	
218-219	Reserved	
220-221	Reserved	
222-223	Reserved	

Table 9-5 loopback requirements

table	byte		value	function
13h	181	media side input loopback	0x00h	loopback disable
			0x01h	loopback enaable
	183	host side input loopback	0x00h	loopback disable
			0x0fh	loopback enaable